## CLAIMS

I CLAIM:

1. A directional ion etching process for patterning self-aligned via contacts comprising:

depositing a photoresist on a patterned layer;

masking the photoresist to provide at least one protected area, the photoresist being developed to remove the photoresist from the non-protected area;

depositing a dielectric coating upon the patterned layer and the remaining photoresist; and

ion etching at a low angle relative to the patterned layer to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact.

2. The process of claim 1, wherein the ion etching is accomplished by a physical ion etching.

3. The process of claim 1, wherein the ion etching is accomplished by a physically assisted process.

4. The process of claim 3, wherein the physically assisted process is reactive ion etching.

5. The process of claim 1, wherein the patterned layer is a magnetic tunnel junction layer.

6. The process of claim 1, further including etching the patterned layer following the developing of the photoresist and prior to the depositing of the dielectric coating.

7. The process of claim 1, wherein the protected area is the intended location of at least one self-aligned via contact.

8. The process of claim 1, wherein the dielectric coated photoresists extend substantially perpendicularly from the surface of the patterned layer, such that the low angle of ion etching relative to the patterned layer is a high angle relative to the extending coated photoresists.

9. The process of claim 1, wherein the via contact exposed by ion etching is in substantially the same plane as the remaining dielectric.

10. The process of claim 1, further including depositing an additional patterned layer and repeating the recited process to establish at least one additional self-aligned contact to the additional patterned layer.

11. The process of claim 10, wherein the additional patterned layer is a conductive layer.

12. A directional ion etching process for patterning self-aligned via contacts, comprising:

depositing a first conductive layer on a wafer substrate;

depositing a junction layer upon the first conductive layer, the junction layer being in electrical contact with the first conductive layer;

depositing a photoresist upon the junction layer;

masking the photoresist to provide a plurality of junction stacks, the photoresist being developed and the exposed junction layer being etched;

depositing a dielectric coating upon the etching exposed surfaces and the photoresist; and

ion etching at a low angle relative to the wafer substrate to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact.

13. The process of claim 12, further including:

depositing a first photoresist layer on the first conductive layer;

masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows;

depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows before the junction layer is deposited.

14. The process of claim 12, wherein the dielectric coating applied to the etching exposed surfaces results in a surface substantially parallel to the wafer substrate, the coated photoresist extending substantially perpendicularly to the wafer substrate, such that the low angle of ion etching relative to the wafer substrate is a high angle relative to the extending coated photoresist.

15. The process of claim 14, wherein the via contact exposed by ion etching is in substantially the same plane as the surface substantially parallel to the wafer substrate.

16. The process of claim 12, wherein the ion etching is accomplished by a physical ion etching.

17. The process of claim 12, wherein the ion etching is accomplished by a physically assisted process.

18. The process of claim 17, wherein the physically assisted process is reactive ion etching.

19. The process of claim 12, wherein the junction stack is a magnetic tunnel junction stack.

20. The process of claim 19, wherein the junction stack comprises a ferromagnetic data layer characterized by an alterable orientation of magnetization, an intermediate layer in contact with the data layer, and a ferromagnetic reference layer in contact with the intermediate layer, opposite from the data layer.

21. The process of claim 12, wherein the self-aligned contacts occur on magnetic memory for use in probe based memory storage systems.

22. The process of claim 12, further including:

depositing an additional patterned layer upon the exposed at least one via contact;

depositing an additional photoresist on the additional patterned layer;

masking the additional photoresist to provide at least one protected area, the additional photoresist being developed to remove the additional photoresist from the non-protected area;

depositing an additional dielectric coating upon the additional patterned layer and the remaining additional photoresist; and

ion etching at a low angle relative to the additional patterned layer to remove the dielectric coated additional photoresist, the removal of the additional photoresist thereby providing at least one self-aligned via contact to the additional patterned layer.

23. The process of claim 22, wherein the additional patterned layer is a conductive layer.

24. A directional ion etching process for patterning self-aligned via contacts comprising:

depositing a first conductive layer upon a wafer substrate;

depositing a first photoresist layer on the first conductive layer;

masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows;

depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows;

depositing a junction layer upon the planarized dielectric, the junction layer being in electrical contact with the conductive rows;

depositing a second photoresist upon the junction layer;

masking the second photoresist to provide a plurality of junction stacks, the second photoresist being developed and the exposed junction layer being etched;

depositing a second dielectric to coat the etching exposed surfaces and the second photoresist; and

ion etching at a low angle relative to the wafer substrate to remove the dielectric coated second photoresist, the removal of the second photoresist thereby providing at least one self-aligned via contact.

25. The process of claim 24, wherein the ion etching is accomplished by a physical ion etching.

26. The process of claim 24, wherein the ion etching is accomplished by a physically assisted process.

27. The process of claim 26, wherein the physically assisted process is reactive ion etching.

28. The process of claim 24, wherein the junction stack is a magnetic tunnel junction stack.

29. The process of claim 28, wherein the junction stack comprises, a ferromagnetic data layer characterized by an alterable orientation of magnetization, an

intermediate layer in contact with the data layer, and a ferromagnetic reference layer in contact with the intermediate layer, opposite from the data layer.

30. The process of claim 24, wherein the first dielectric is planarized by CMP planarization.

31. The process of claim 24, wherein the second dielectric coating applied to the etching exposed surfaces results in a surface substantially parallel to the wafer substrate, the coated second photoresist extending substantially perpendicularly to the wafer substrate, such that the low angle of ion etching relative to the wafer substrate is a high angle relative to the extending coated second photoresist.

32. The process of claim 24, wherein the thickness of the second dielectric coating is substantially the height of the junction stacks, such that the top surface of the dielectric coating is in substantially the same plane as the top of the junction stacks.

33. The process of claim 24, wherein the via contact exposed by ion etching is in substantially the same plane as the surface substantially parallel to the wafer substrate.

34. The process of claim 24, wherein the self-aligned contacts occur on magnetic memory for use in probe based memory storage systems.

35. The process of claim 24, further including:

depositing a second conductive layer upon the exposed via contacts;

depositing a third photoresist layer on the second conductive layer; and

masking the third photoresist layer to provide conductive columns transverse to the conductive rows, the third photoresist being developed, the exposed second conductive layer being etched and the remaining third photoresist being dissolved to expose the conductive columns.

36. The process of claim 35, wherein the self-aligned contacts occur on magnetic memory for use in cross-point magnetic memory array applications.

37. The process of claim 24, further including:

depositing an additional patterned layer upon the exposed at least one via contact;

depositing an additional photoresist on the additional patterned layer;

masking the additional photoresist to provide at least one protected area, the

additional photoresist being developed to remove the additional photoresist from the non-protected area;

depositing an additional dielectric coating upon the additional patterned layer and the remaining additional photoresist; and

ion etching at a low angle relative to the additional patterned layer to remove the dielectric coated additional photoresist, the removal of the additional photoresist thereby providing at least one self-aligned via contact to the additional patterned layer.

38. The process of claim 37, wherein the additional patterned layer is a conductive layer.